

# DATA SHEET

## **74AVC16834A**

18-bit registered driver  
with inverted register enable and  
Dynamic Controlled Outputs™ (3-State)

Product data  
Supersedes data of 2000 Jul 25

2002 Sep 11

# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

74AVC16834A

## FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A/5/7
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- DCO (Dynamic Controlled Output) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Power off disables 74AVC16834A outputs, permitting Live Insertion
- Integrated input diodes to minimize input overshoot and undershoot
- Full PC133 solution provided when used with PCK2509S or PCK2510S and CBT16292

## DESCRIPTION

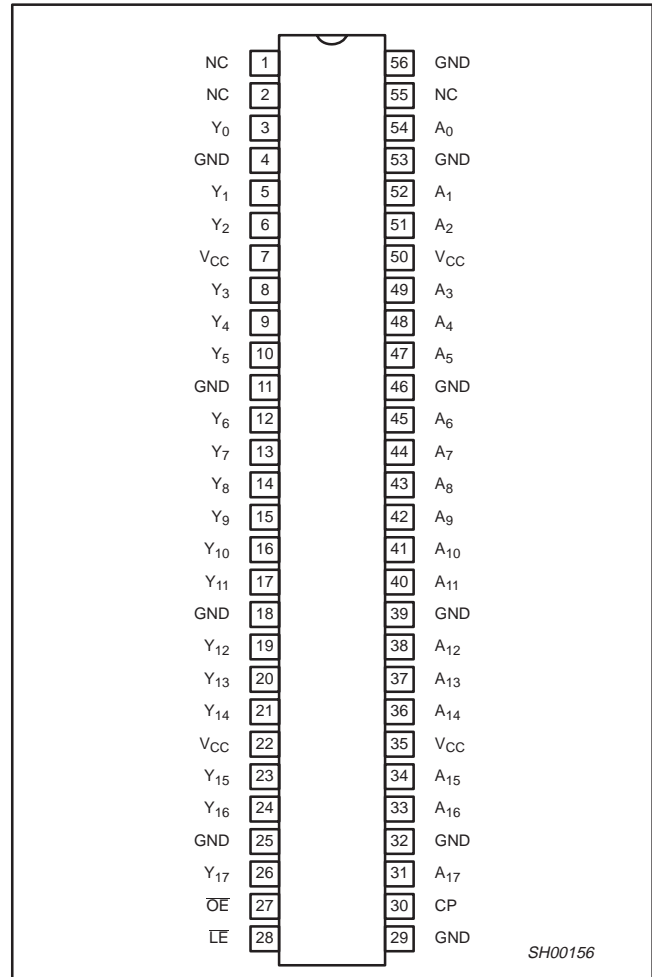
The 74AVC16834A is a 18-bit universal bus driver. Data flow is controlled by output enable ( $\overline{OE}$ ), latch enable ( $\overline{LE}$ ) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See the graphs on page 9 for typical curves.

## PIN CONFIGURATION



SH00156

## QUICK REFERENCE DATA

$GND = 0 V$ ;  $T_{amb} = 25\text{ }^{\circ}C$ ;  $t_r = t_f \leq 2.0\text{ ns}$ ;  $C_L = 30\text{ pF}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay An to Yn	$V_{CC} = 1.8\text{ V}$ $V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$	2.6 2.0 1.7	ns
$t_{PHL}/t_{PLH}$	Propagation delay LE to Yn; CP to Yn	$V_{CC} = 1.8\text{ V}$ $V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$	2.9 2.3 1.9	ns
$C_I$	Input capacitance		5.0	pF
$C_{PD}$	Power dissipation capacitance per buffer	$V_I = GND\text{ to }V_{CC}^1$	Outputs enabled 25 Output disabled 6	pF

### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic 0.5 mm pitch TSSOP	$-40^{\circ}C$ to $+85^{\circ}C$	74AVC16834ADGG	SOT364-1
56-Pin Plastic 0.4 pitch TSSOP (TVSOP)	$-40^{\circ}C$ to $+85^{\circ}C$	74AVC16834ADGV	SOT481-2

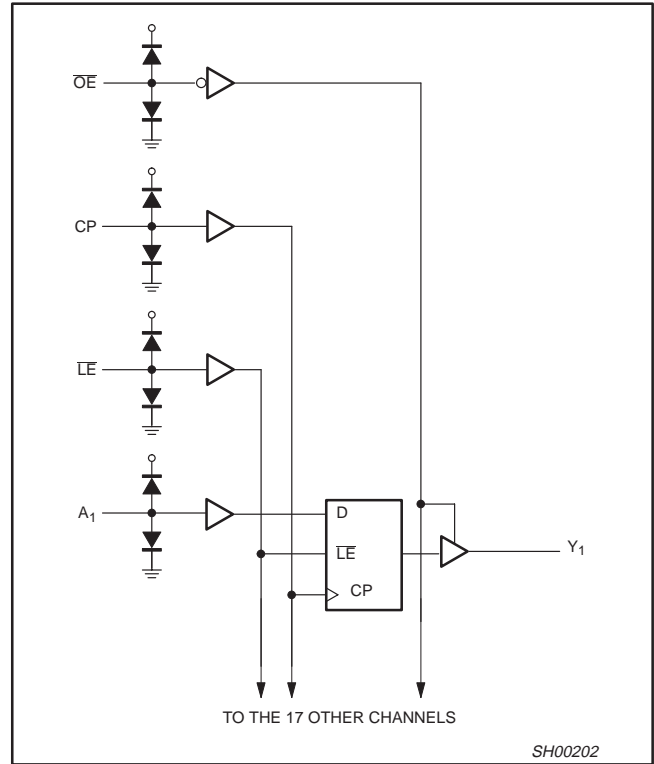
# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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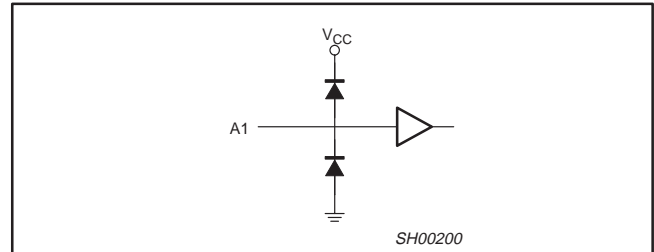
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y <sub>0</sub> to Y <sub>17</sub>	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0 V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage
27	$\overline{OE}$	Output enable input (active LOW)
28	$\overline{LE}$	Latch enable input (active LOW)
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A <sub>0</sub> to A <sub>17</sub>	Data inputs

## LOGIC SYMBOL



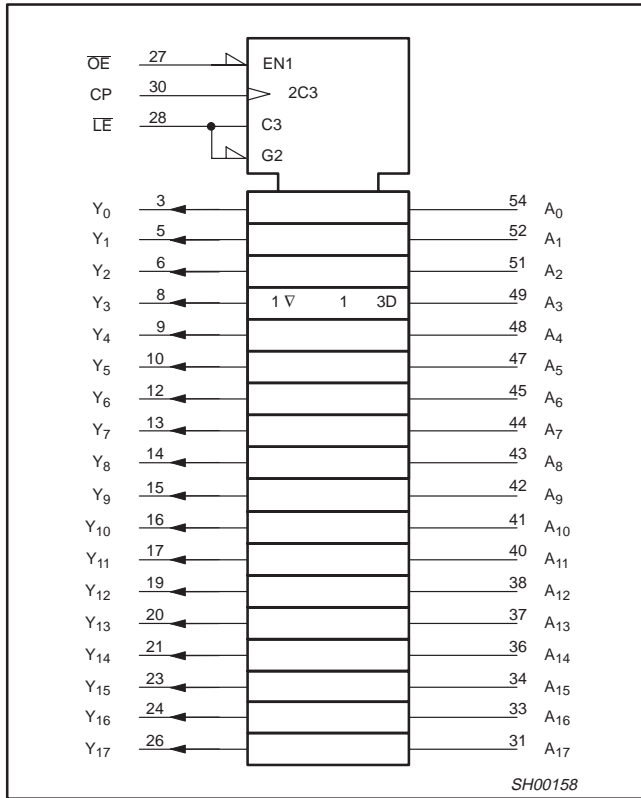
## TYPICAL INPUT (DATA OR CONTROL)



# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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## LOGIC SYMBOL (IEEE/IEC)



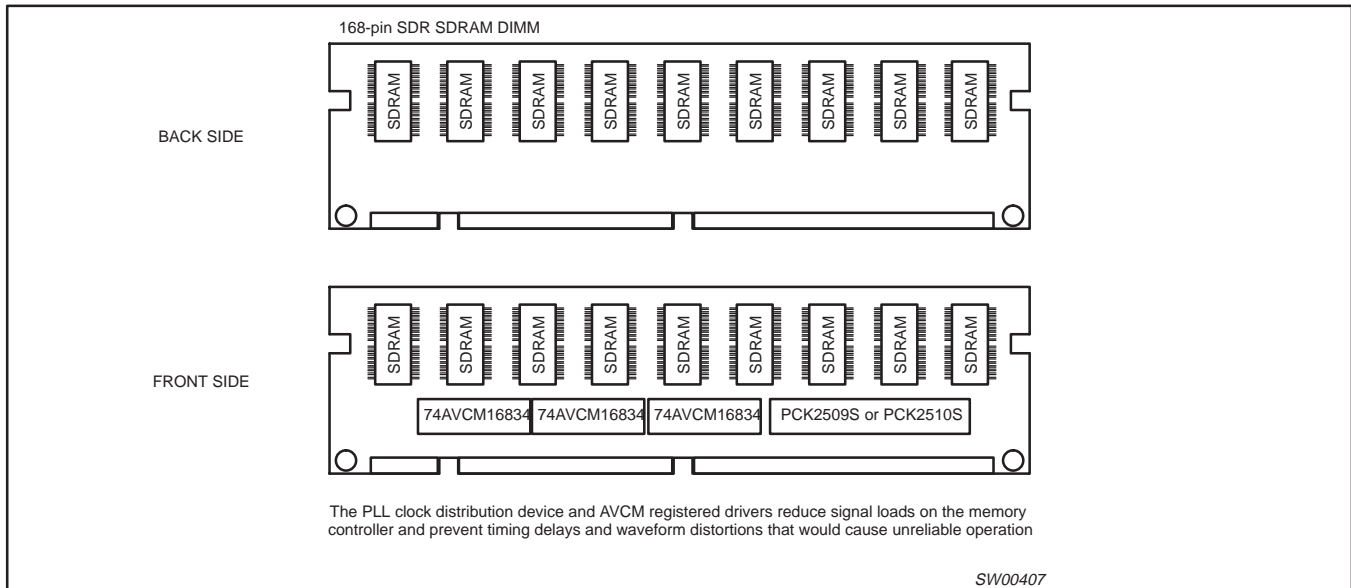
## FUNCTION TABLE

INPUTS				OUTPUTS
OE	LE	CP	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y <sub>0</sub> <sup>1</sup>
L	H	L	X	Y <sub>0</sub> <sup>2</sup>

H = HIGH voltage level  
 L = LOW voltage level  
 X = Don't care  
 Z = High impedance "off" state  
 ↑ = LOW-to-HIGH level transition

### NOTES:

- Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
- Output level before the indicated steady-state input conditions were established.



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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
$V_{CC}$	DC supply voltage (according to JEDEC Low Voltage Standards)		1.65 2.3 3.0	1.95 2.7 3.6	V
	DC supply voltage (for low voltage applications)		1.2	3.6	V
$V_I$	DC Input voltage range		0	3.6	V
$V_O$	DC output voltage range; output 3-State		0	3.6	V
	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_p, t_f$	Input rise and fall times	$V_{CC} = 1.65$ to $2.3$ V	0	30	ns/V
		$V_{CC} = 2.3$ to $3.0$ V	0	20	
		$V_{CC} = 3.0$ to $3.6$ V	0	10	

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For all inputs <sup>1</sup>	-0.5 to 4.6	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage; output 3-State	Note 1	-0.5 to 4.6	V
$V_O$	DC output voltage; output HIGH or LOW state	Note 1	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55 °C derate linearly with 8 mW/K	600	mW

### NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	–	–	V
		V <sub>CC</sub> = 1.65 to 1.95 V	0.65V <sub>CC</sub>	0.9	–	
		V <sub>CC</sub> = 2.3 to 2.7 V	1.7	1.2	–	
		V <sub>CC</sub> = 3.0 to 3.6 V	2.0	1.5	–	
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2 V	–	–	GND	V
		V <sub>CC</sub> = 1.65 to 1.95 V	–	0.9	0.35V <sub>CC</sub>	
		V <sub>CC</sub> = 2.3 to 2.7 V	–	1.2	0.7	
		V <sub>CC</sub> = 3.0 to 3.6 V	–	1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 1.65 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100 μA	V <sub>CC</sub> - 0.20	V <sub>CC</sub>	–	V
		V <sub>CC</sub> = 1.65 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -4 mA	V <sub>CC</sub> - 0.45	V <sub>CC</sub> - 0.10	–	
		V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -8 mA	V <sub>CC</sub> - 0.55	V <sub>CC</sub> - 0.28	–	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12 mA	V <sub>CC</sub> - 0.70	V <sub>CC</sub> - 0.32	–	
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 1.65 to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 μA	–	GND	0.20	V
		V <sub>CC</sub> = 1.65 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4 mA	–	0.10	0.45	
		V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	–	0.26	0.55	
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12 mA	–	0.36	0.70	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 1.65 to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	–	0.1	2.5	μA
I <sub>OFF</sub>	3-State output OFF-state current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 3.6 V	–	0.1	± 10	μA
I <sub>IHZ</sub> /I <sub>ILZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 1.65 to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	–	0.1	12.5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 1.65 to 2.7 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	–	0.1	5	μA
		V <sub>CC</sub> = 3.0 to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	–	0.1	10	
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 1.65 to 2.7 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	–	0.1	20	μA
		V <sub>CC</sub> = 3.0 to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	–	0.2	40	

### NOTE:

1. All typical values are at T<sub>amb</sub> = 25 °C.

# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.0$  ns;  $C_L = 30$  pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS												UNIT	
			$V_{CC} = 3.3 \pm 0.3$ V			$V_{CC} = 2.5 \pm 0.2$ V			$V_{CC} = 1.8 \pm 0.15$ V			$V_{CC} = 1.5 \pm 0.1$ V		$V_{CC} = 1.5$ V		$V_{CC} = 1.2$ V
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP		TYP
$t_{PHL}/t_{PLH}$	Propagation delay An to Yn	1, 7	0.9 0.7	1.7	2.6 2.5	1.0 0.8	2.0	3.2 3.0	1.5 1.0	2.8 2.6	4.9 4.5	2.0	5.8	3.6	5.9 5.2	ns
	Propagation delay $\overline{LE}$ to Yn	2, 7	1.2 0.7	2.0 1.9	3.0 2.9	1.5 0.8	2.4 2.3	3.7 3.5	1.8 1.0	3.4 2.9	5.3	2.3	6.5	4.0	6.5 5.8	
	Propagation delay CP to Yn	3, 7	0.8 0.7	1.7	2.5	1.1 0.8	2.0	3.0	1.6 1.0	2.8 2.6	4.4 4.5	2.0	5.1	3.7	4.9 5.2	
$t_{PZH}/t_{PZL}$	3-State output enable time OE to Yn	6, 7	1.3 1.0	2.5 2.3	4.3 4.0	1.6 1.0	2.8 2.5	4.8 4.5	2.2 1.5	4.0 3.0	6.7 6.5	2.8	8.2	5.0	8.0 5.5	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time OE to Yn	6, 7	1.5 1.0	3.0 2.3	4.7 3.5	1.5 1.0	3.4 2.2	5.6 4.0	2.4 1.5	4.6 3.5	7.2 6.5	2.1	6.9	4.5	6.5 5.5	ns
$t_w$	CP pulse width HIGH or LOW	3, 7	1.0	–	–	1.2	–	–	2.0	–	–	–	–	–	–	ns
	$\overline{LE}$ pulse width HIGH	2, 7	1.0	–	–	1.2	–	–	2.0	–	–	–	–	–	–	
$t_{SU}$	Set-up time An to CP	5, 7	0.3	–0.5	–	0.1	–0.2	–	0	–0.2	–	0.2	–	0	0	ns
	Set-up time An to $\overline{LE}$	4, 7	0.5	0.1	–	0.6	0.1	–	1.0	0.5	–	1.5	–	0.8	1.5	
$t_h$	Hold time An to CP	5, 7	0.9	0.6	–	0.7	0.3	–	0.7	0.3	–	0.6	–	0.3	0.1	ns
	Hold time An to $\overline{LE}$	4, 7	0.6	0.4	–	0.2	0.1	–	0.1	0	–	0.1	–	0	–0.7	
$f_{max}$	Maximum clock pulse frequency	3, 7	500	–	–	400	–	–	250	–	–	–	–	–	–	MHz

### NOTE:

1. All typical values are measured at  $T_{amb} = 25$  °C and at  $V_{CC} = 1.8$  V, 2.5 V, 3.3 V.

# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

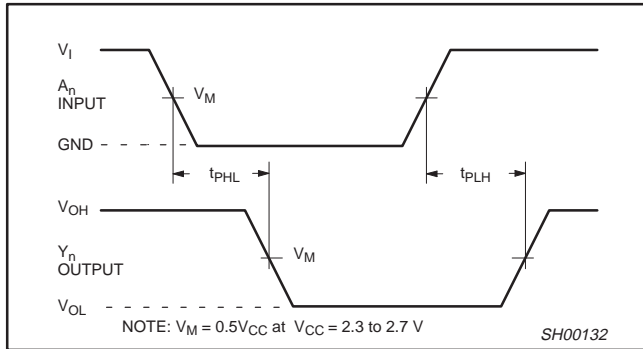
74AVC16834A

## AC WAVEFORMS FOR $V_{CC} = 3.0\text{ V TO } 3.6\text{ V RANGE}$

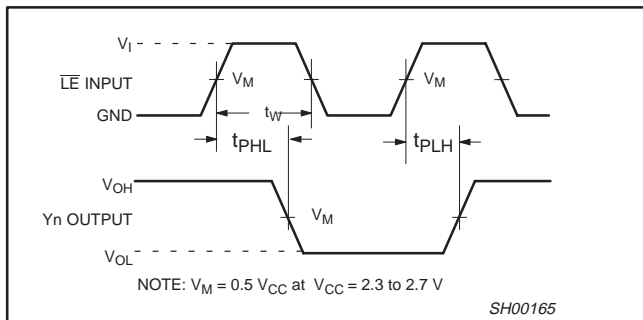
$V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.300\text{ V}$   
 $V_Y = V_{OH} - 0.300\text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$

## AC WAVEFORMS FOR $V_{CC} = 2.3\text{ V TO } 2.7\text{ V AND } V_{CC} < 2.3\text{ V RANGE}$

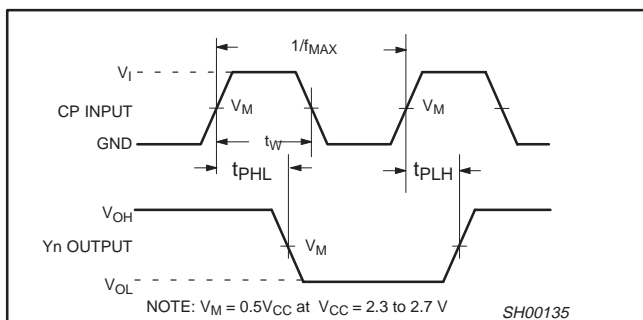
$V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.15\text{ V}$   
 $V_Y = V_{OH} - 0.15\text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$



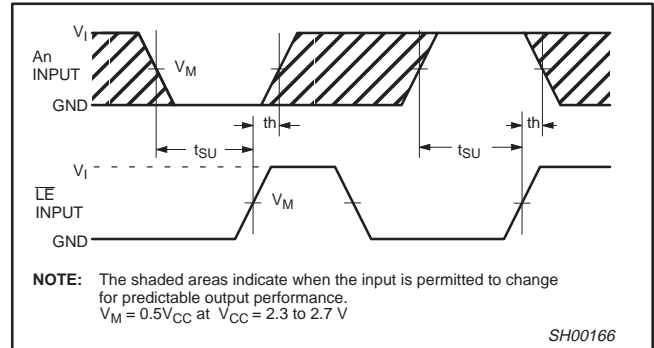
Waveform 1. Input (An) to output (Yn) propagation delay



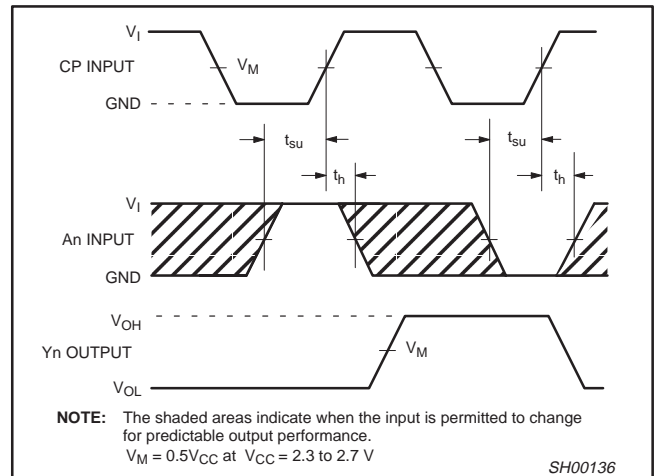
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



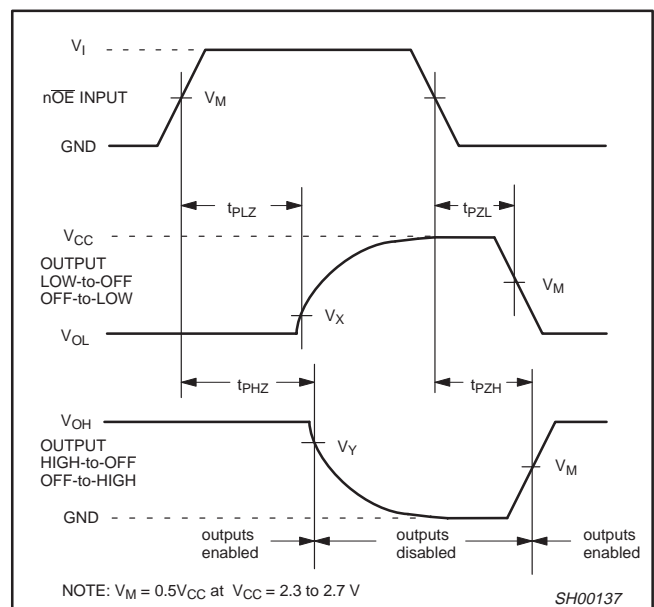
Waveform 3. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.



Waveform 4. Data set-up and hold times for the An input to the LE input



Waveform 5. Data set-up and hold times for the An input to the clock CP input



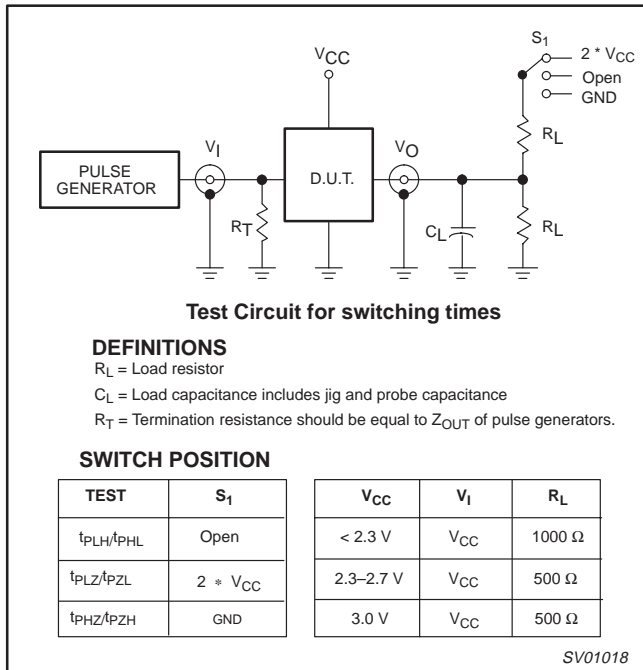
Waveform 6. 3-State enable and disable times



# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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## TEST CIRCUIT



Waveform 7. Load circuitry for switching times

## GRAPHS

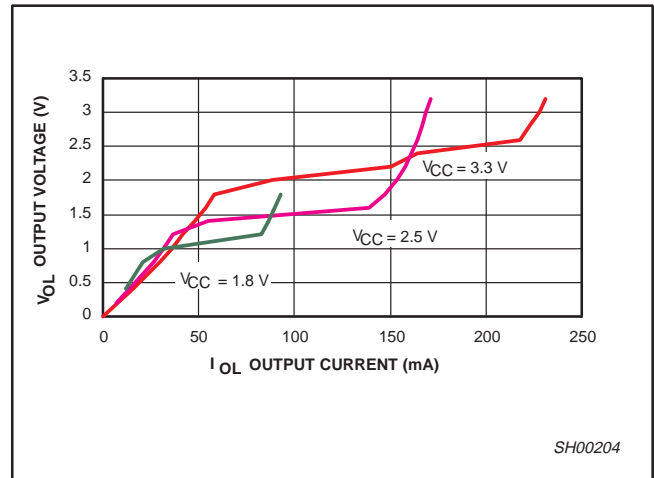


Figure 1. Output voltage ( $V_{OL}$ ) vs. output current ( $I_{OL}$ )

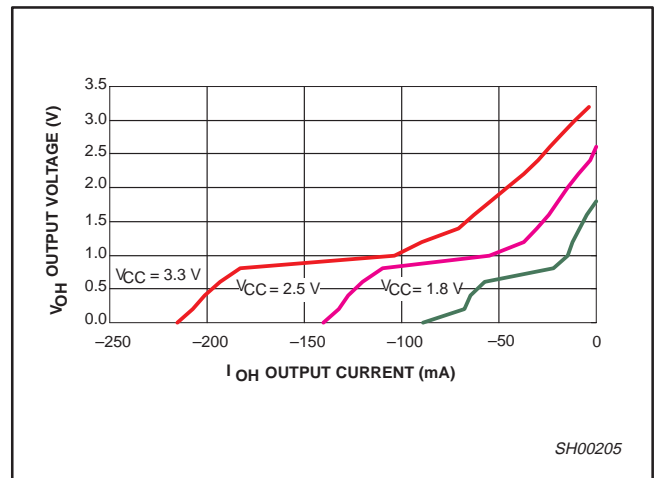


Figure 2. Output voltage ( $V_{OH}$ ) vs. output current ( $I_{OH}$ )

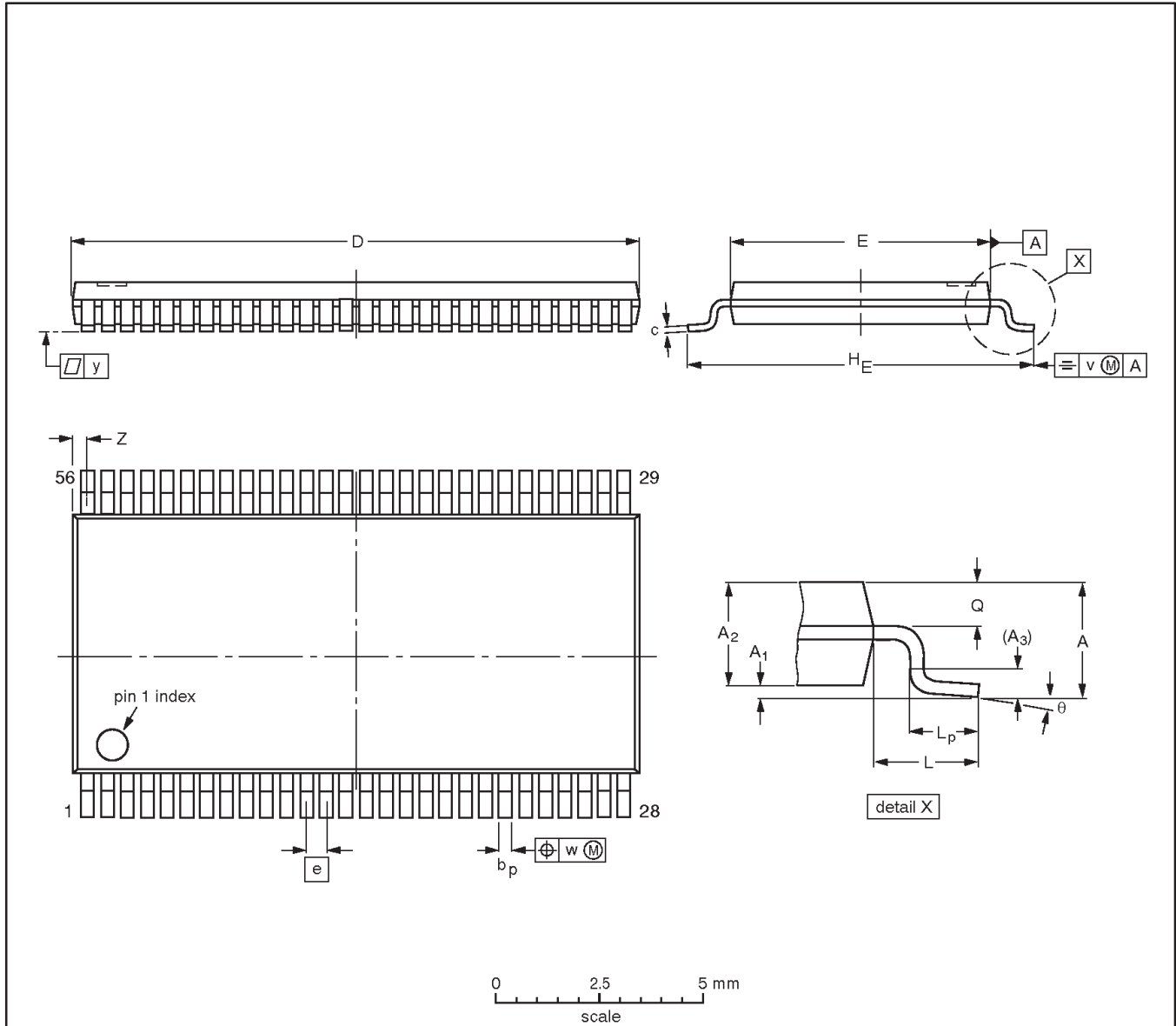
A Dynamic Controlled Output (DCO) circuit is designed in. During the transition, it initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figures 1 and 2 show  $V_{OL}$  vs.  $I_{OL}$  and  $V_{OH}$  vs.  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DCO circuit provides a maximum dynamic drive that is equivalent to a high drive standard output device.

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

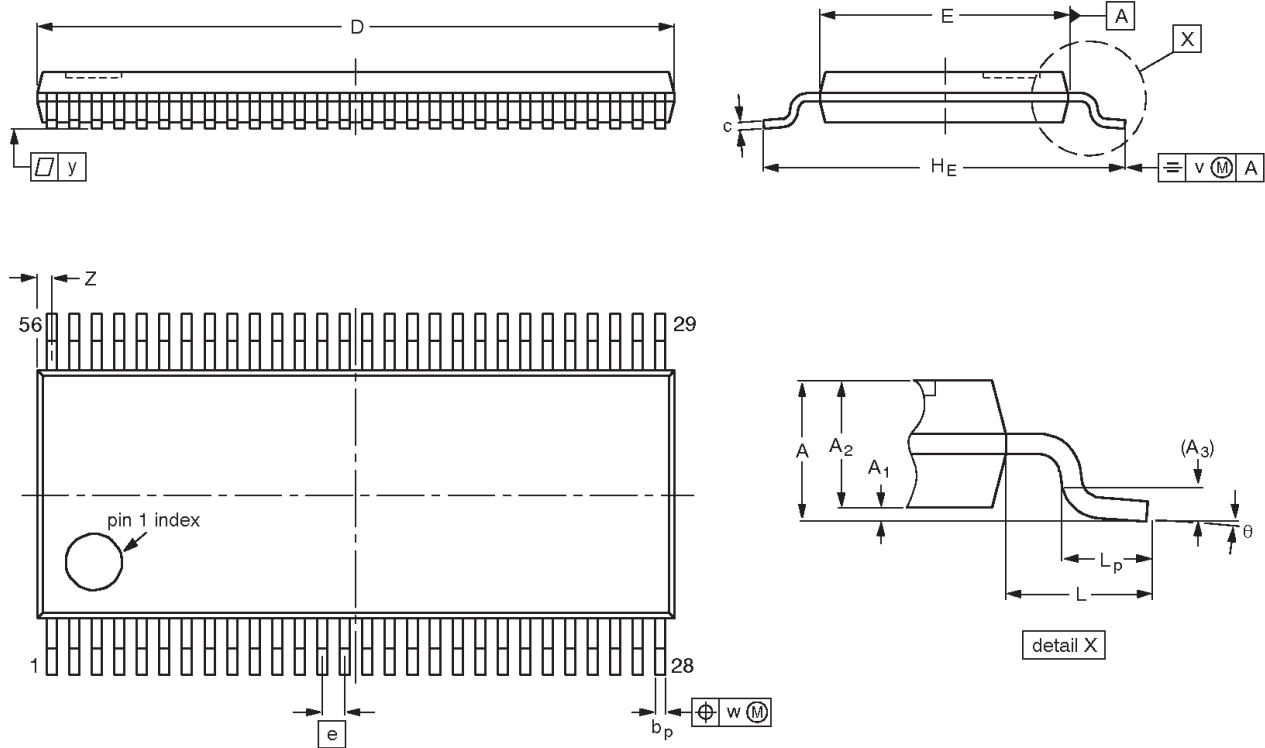
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				95-02-10 99-12-27

18-bit registered driver with inverted register enable  
and Dynamic Controlled Outputs™ (3-State)

74AVC16834A

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 4.4 mm

SOT481-2



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D (1)	E (2)	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z (1)	θ
mm	1.2	0.15 0.05	1.05 0.80	0.25	0.23 0.13	0.20 0.09	11.4 11.2	4.5 4.3	0.4	6.6 6.2	1	0.75 0.45	0.2	0.07	0.08	0.4 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT481-2	---	MO-194	---			01-11-24

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**18-bit registered driver with inverted register enable  
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**REVISION HISTORY**

<b>Rev</b>	<b>Date</b>	<b>Description</b>
_4	2000 Jul 25	Product specification (9397 750 07353); fourth version. Engineering Change Notice: 853-2207 24201:
_5	2002 Sep 11	Product data (9397 750 10331); fifth version supersedes Product specification 2000 Jul 25. Engineering Change Notice: 853-2207 28874 (2002 Sep 09). Modifications: Add new package option (TVSOP) to existing product data sheet.

# 18-bit registered driver with inverted register enable and Dynamic Controlled Outputs™ (3-State)

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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